REMARKS/ARGUMENTS

The present Amendment is in response to the Office Action mailed December 7, 2001 in the above-identified patent application. Enclosed herewith is a Petition requesting a two-month extension of time for extending the deadline for responding to the Office Action from March 7, 2002, to and including May 7, 2002.

The Examiner rejected claim 48 under 35 U.S.C. § 112, first paragraph, as containing subject matter that was not described in the specification. In response, Applicants have amended claim 48 to recite that the step of selectively forming bond ribbons includes "depositing a conductive material over the top of said package and etching away portions of said conductive material." Support for this recitation is found in the specification at, *inter alia*, page 14, lines 15-21. In view of the above-noted amendment to Claim 48, Applicants respectfully assert that claim 48 now satisfies the requirements of 35 U.S.C. § 112, first paragraph, and is otherwise allowable.

Citing 35 U.S.C. § 132, the Examiner objected to the Amendment filed October 1, 2001 as introducing new matter. In view of the above noted amendment to claim 48, Applicants respectfully assert that the Examiner's objection has been rendered moot.

The Examiner rejected claims 36-44 under 35 U.S.C. § 112, second paragraph, as being indefinite. Specifically, the Examiner noted that Claims 36-44 depend on cancelled claims 1 and 4. In response, Applicants have amended claims 36-44 to depend either directly or indirectly from claim 35. In view of the above-noted amendments to claims 36-44, Applicants respectfully assert that claims 36-44 now satisfy the requirements of 35 U.S.C. § 112, second paragraph.

Claims 35, 46-47, 49-54 and 57 are rejected under 35

U.S.C. § 102(b) as being anticipated by U.S. Patent 5,070,297 to *Kwon et al.*, or, in the alternative, under 35 U.S.C. § 103(a) as obvious over *Kwon* and U.S. Patent 4,671,849 to *Chen*.

Referring to FIGS. 4A-4H thereof, *Kwon* discloses a method of making an integrated circuit testing device including providing a silicon substrate 38, an active element 36 atop the silicon substrate 38, a silicone dioxide layer 34 over the active element 36, and a compliant layer atop the silicone dioxide layer 34. Referring to FIG. 4B, vias are formed in the compliant layer 32 and the silicone dioxide layer 34 to expose portions of the active element 36. Each via defines a conical-shaped opening extending between top and bottom surfaces of compliant layer 32. A conductive coating 30 and a metal contact layer 28 are then deposited within the via openings, as shown in FIG. 4C. Referring to FIG. 4D, a compliant protective coating 26 is then formed atop compliant layer 32, metal contact layer 28 and conductive coating 30. The compliant protective coating 26 is etched to form openings extending to metal contact layer 28, and a seed layer is sputtered over the protective coating 26 to form a connector base in each opening in the protective coating 26. A conductive metal layer is then sputtered over connector base 24 to form connector caps 22. Referring to FIGS. 4F-4H, test probes 16 are then attached to the assembly and electrically interconnected with the conductive metal 28, 30 in the vias. In sum, *Kwon* teaches making metalized vias by first forming via openings in a compliant layer and then depositing one or more layers of conductive material in the via openings. The via openings are defined by steep sloping sidewalls having acute edges at the top and bottom surfaces of the compliant layer 32. As a result, the conductive coating 30 deposited in the via has sharp edges at the top and bottom surfaces of the compliant layer 32.

Referring to FIG. 8 thereof, *Chen* discloses a

structure including an insulating layer 10 having a curved transition region at a top surface thereof and an acute edge at a bottom surface thereof.

In contrast to *Kwon* and *Chen*, the present application is directed to methods of forming elongated bond ribbons over a compliant layer. The compliant layer has curved transition regions at the top and bottom surfaces thereof so that the elongated bond ribbons formed over the compliant layer have no sharp edges or kinks that may result in weakening of the bond ribbons. As a result, the bond ribbons are more reliable during operation and thermal cycling.

Claim 35 patentable over *Kwon* and *Chen* because the references neither disclose nor suggest "providing a compliant layer over said dielectric protective layer..., wherein said compliant layer has a substantially flat top surface, a bottom surface that is attached to said dielectric protective layer and sloping edges between the top surface and the bottom surface, wherein the sloping edges of said compliant layer have a first curved transition region near the top surface of said compliant layer and a second curved transition region near the bottom surface of said complaint layer." (Emphasis added) Clearly, *Kwon's* compliant layer 32 (FIG. 2) does not have curved transition regions near the top and bottom surfaces thereof, a limitation explicitly recited in claim 35.

Claim 35 is also patentable over *Kwon* and *Chen* because the references neither disclose nor suggest "selectively electroplating elongated bond ribbons atop said dielectric protective layer and said compliant layer." The conductive metal layers 28, 30 deposited in *Kwon's* via openings do not form "elongated bond ribbons." Rather, *Kwon's* metalized vias have a "V" or conical-shaped cross section that teaches away from Applicants' claimed "elongated bond ribbons." Claim 35 is also patentable because the references neither disclose nor suggest

that the "elongated bond ribbons... have a first curved region overlying the first curved transition region of said compliant layer and a second curved region overlying the second curved transition region of said compliant layer." For all of these reasons, claim 35 is unanticipated by *Kwon* and is otherwise allowable.

Claim 45 is patentable over *Kwon* and *Chen* because the cited references neither disclose nor suggest a method of making a compliant microelectronic package including providing a compliant layer, "wherein the sloping edges of said compliant layer have first curved transition regions near the top surface of said compliant layer and second curved transition regions near the bottom surface of said compliant layer." Claim 45 is also patentable because the cited references neither disclose nor suggest the step of "selectively forming elongated, flexible bond ribbons over the top surface and the sloping edge surfaces of said compliant layer..., wherein said elongated, flexible bond ribbons extending along the sloping edges of said compliant layer have first curved regions overlying the first curved transition regions of said compliant layer and second curved regions overlying the second curved transition regions of said compliant layer." Claims 46-54 and 57 are also patentable, *inter alia*, by virtue of their dependence either directly or indirectly from claim 45, which is patentable for the reasons set forth above.

The Examiner rejected claim 48 under 35 U.S.C. § 103(a) as being unpatenable over *Kwon*, or, in the alternative, over the combination of *Kwon* and *Chen*, and further in view of U.S. Patent 4,935,312 to *Nakayama*. A review of *Nakayama* indicates that it does not overcome the deficiencies noted above in *Kwon* and *Chen*. As such, Applicants respectfully assert that claim 48 is patentable over the references cited by the Examiner, *inter alia*, by virtue of its dependence from claim 45,

which is patentable for the reasons set forth above.

Claims 55 and 56 are also rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kwon* and U.S. Patent 5,874,782 to *Palagonia*. Referring to FIGS. 3A and 5 thereof, *Palagonia* teaches a method for separating adjacent semiconductor chip packages 22 from one another. *Palagonia*, however, does not overcome the deficiencies noted above in *Kwon*. Thus, claims 55 and 56 are patentable over the combination of *Kwon* and *Palagonia*, *inter alia*, by virtue of their dependence from claim 45, which is allowable for the reasons set forth above.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he telephone Applicants' attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

If there are any additional charges in connection with this requested Amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

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Respectfully submitted,

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Version With Markings to Show Changes Made

36. (Amended) The method according to Claim ~~1~~ 35, further comprising after selectively electroplating said bond ribbons, providing a second dielectric protective layer over exposed elements on the terminal side of said package, wherein said second dielectric protective layer has a plurality of apertures extending therethrough for providing access to said terminals.

37. (Amended) The method according to Claim ~~1~~ 35, wherein said compliant layer comprises a material selected from the group consisting of silicone, flexibilized epoxy, a thermosetting polymer, fluoropolymer, thermoplastic polymer, polyimide, foams and combinations or composites thereof.

38. (Amended) The method according to Claim ~~1~~ 35, further including the step of providing an encapsulant layer atop an exposed surface of said bond ribbons.

39. (Amended) The method according to Claim ~~4~~ 38, wherein the encapsulant layer material is selected from the group consisting of silicone, flexibilized epoxy, thermoplastic and gel.

40. (Amended) The method according to Claim ~~4~~ 38, further including the step of providing a second dielectric layer atop said encapsulant layer, wherein said second dielectric layer has a plurality of apertures for providing access to said terminals.

41. (Amended) The method according to Claim ~~1~~ 35, wherein said dielectric layer is a silicon dioxide passivation layer provided on the contact bearing surface of said semiconductor chip.

42. (Amended) The method according to Claim ~~1~~ 35, further including before providing the compliant layer, plating a barrier metal atop the contacts of said semiconductor chip, wherein said barrier metal reduces voiding at an interface between the contacts and said bond ribbons.

43. (Amended) The method according to Claim ~~1~~ 35, wherein the method steps are applied simultaneously to a plurality of undiced semiconductor chips on a wafer to form a plurality of compliant semiconductor chip packages, the method further including dicing said wafer after selectively electroplating said bond ribbons to provide a plurality of individual compliant semiconductor chip packages.

44. (Amended) The method according to Claim ~~1~~ 35, wherein the method steps are applied simultaneously to a plurality of adjacent semiconductor chips arranged in an array to form a plurality of compliant semiconductor chip packages, the method further including the step of dicing said adjacent packages after selectively electroplating said bond ribbons to provide a plurality of individual compliant semiconductor chip packages.

48. (Amended) The method as claimed in claim 45, wherein said selectively forming bond ribbons step includes ~~electrolessly plating~~ depositing a conductive material over the top of said package and ~~selectively~~ etching away portions of said conductive material.

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